# 8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

# 74HC/HCT595

## FEATURES

- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- 100 MHz (typ) shift out frequency
- Output capability:
  - parallel outputs; bus driver
  - serial output; standard
- $I_{CC}$ category: MSI.

## APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register.

## DESCRIPTION

The 74HC/HCT595 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The “595” is an 8-stage serial shift register with a storage register and 3-state outputs. The shift register and storage register have separate clocks.

Data is shifted on the positive-going transitions of the $SH_{CP}$ input. The data in each register is transferred to the storage register on a positive-going transition of the $ST_{CP}$ input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input ($D_S$) and a serial standard output ($Q_7$’) for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input (OE) is LOW.

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25 °C; $t_r = t_f$ = 6 ns.

| SYMBOL | PARAMETER | CONDITIONS | TYP. | | UNIT |
|---|---|---|---|---|---|
| | | | HC | HCT | |
| $t_{PHL}/t_{PLH}$ | propagation delay | $C_L$ = 15 pF; $V_{CC}$ = 5 V | | | |
| | $SH_{CP}$ to $Q_7$’ | | 16 | 21 | ns |
| | $ST_{CP}$ to $Q_n$ | | 17 | 20 | ns |
| | $\overline{MR}$ to $Q_7$’ | | 14 | 19 | ns |
| $f_{max}$ | maximum clock frequency $SH_{CP}$, $ST_{CP}$ | | 100 | 57 | MHz |
| $C_I$ | input capacitance | | 3.5 | 3.5 | pF |
| $C_{PD}$ | power dissipation capacitance per package | notes 1 and 2 | 115 | 130 | pF |

**Notes**

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   $f_i$ = input frequency in MHz

   $f_o$ = output frequency in MHz

   $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   $C_L$ = output load capacitance in pF

   $V_{CC}$ = supply voltage in V
2. For HC the condition is $V_I$ = GND to $V_{CC}$; for HCT the condition is $V_I$ = GND to $V_{CC}$ – 1.5 V.

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| 74HC595N | DIP16 | plastic dual in-line package; 16 leads (300 mil); long body | SOT38-1 |
| 74HC595D | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74HC595DB | SSOP16 | plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |
| 74HC595PW | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74HCT595N | DIP16 | plastic dual in-line package; 16 leads (300 mil); long body | SOT38-1 |
| 74HCT595D | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |

## PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| $Q_0$ to $Q_7$ | 15, 1 to 7 | parallel data output |
| GND | 8 | ground (0 V) |
| $Q_7$' | 9 | serial data output |
| $\overline{MR}$ | 10 | master reset (active LOW) |
| $SH_{CP}$ | 11 | shift register clock input |
| $ST_{CP}$ | 12 | storage register clock input |
| $\overline{OE}$ | 13 | output enable (active LOW) |
| $D_S$ | 14 | serial data input |
| $V_{CC}$ | 16 | positive supply voltage |

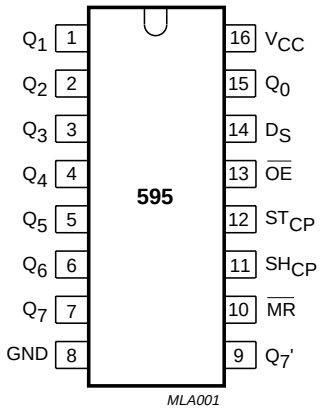



Fig.1 Pin configuration.

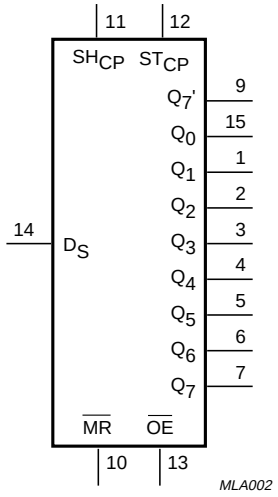



Fig.2 Logic symbol.

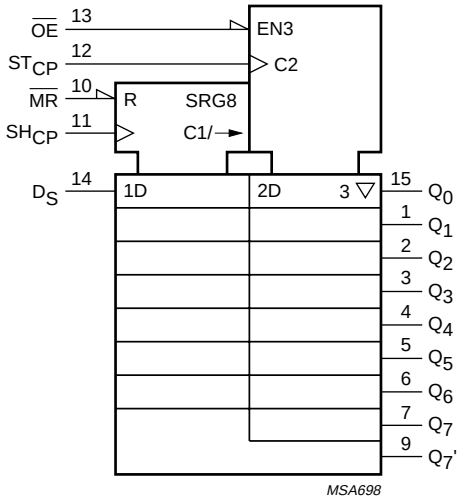



Fig.3 IEC logic symbol.

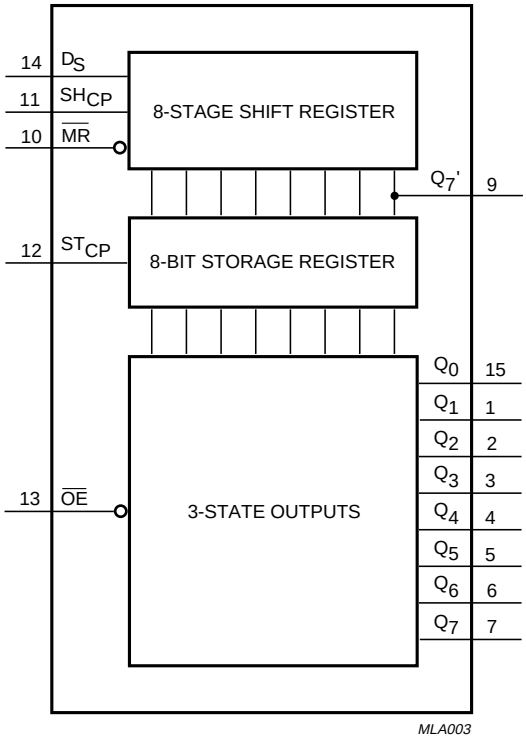



Fig.4 Functional diagram.

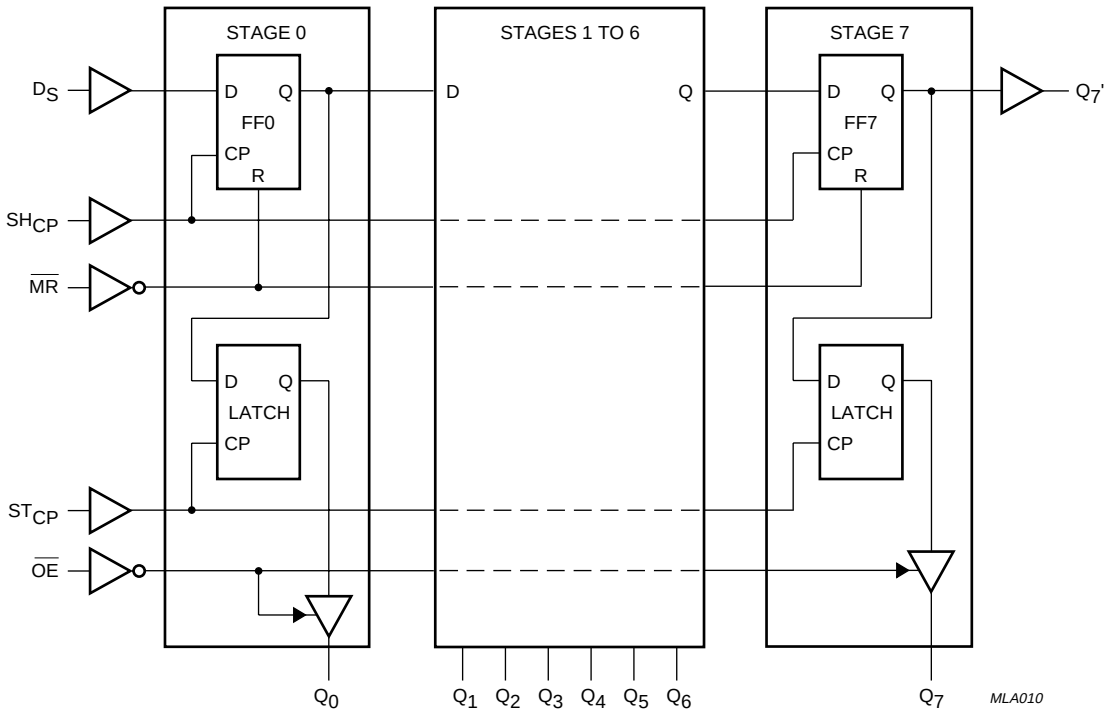



Fig.5 Logic diagram.

**FUNCTION TABLE**

| INPUTS | | | | | OUTPUTS | | FUNCTON |
|---|---|---|---|---|---|---|---|
| $SH_{CP}$ | $ST_{CP}$ | $\overline{OE}$ | $\overline{MR}$ | $D_S$ | $Q_7$' | $Q_N$ | |
| X | X | L | L | X | L | NC | a LOW level on $\overline{MR}$ only affects the shift registers |
| X | ↑ | L | L | X | L | L | empty shift register loaded into storage register |
| X | X | H | L | X | L | Z | shift register clear. Parallel outputs in high-impedance OFF-state |
| ↑ | X | L | H | H | $Q_6$' | NC | logic high level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal $Q_6$') appears on the serial output ($Q_7$') |
| X | ↑ | L | H | X | NC | $Q_n$' | contents of shift register stages (internal $Q_n$') are transferred to the storage register and parallel output stages |
| ↑ | ↑ | L | H | X | $Q_6$' | $Q_n$' | contents of shift register shifted through. Previous contents of the shift register is transferred to the storage register and the parallel output stages. |

**Notes**

1. H = HIGH voltage level; L = LOW voltage level
   ↑ = LOW-to-HIGH transition; ↓ = HIGH-to-LOW transition
   Z = high-impedance OFF-state; NC = no change
   X = don't care.

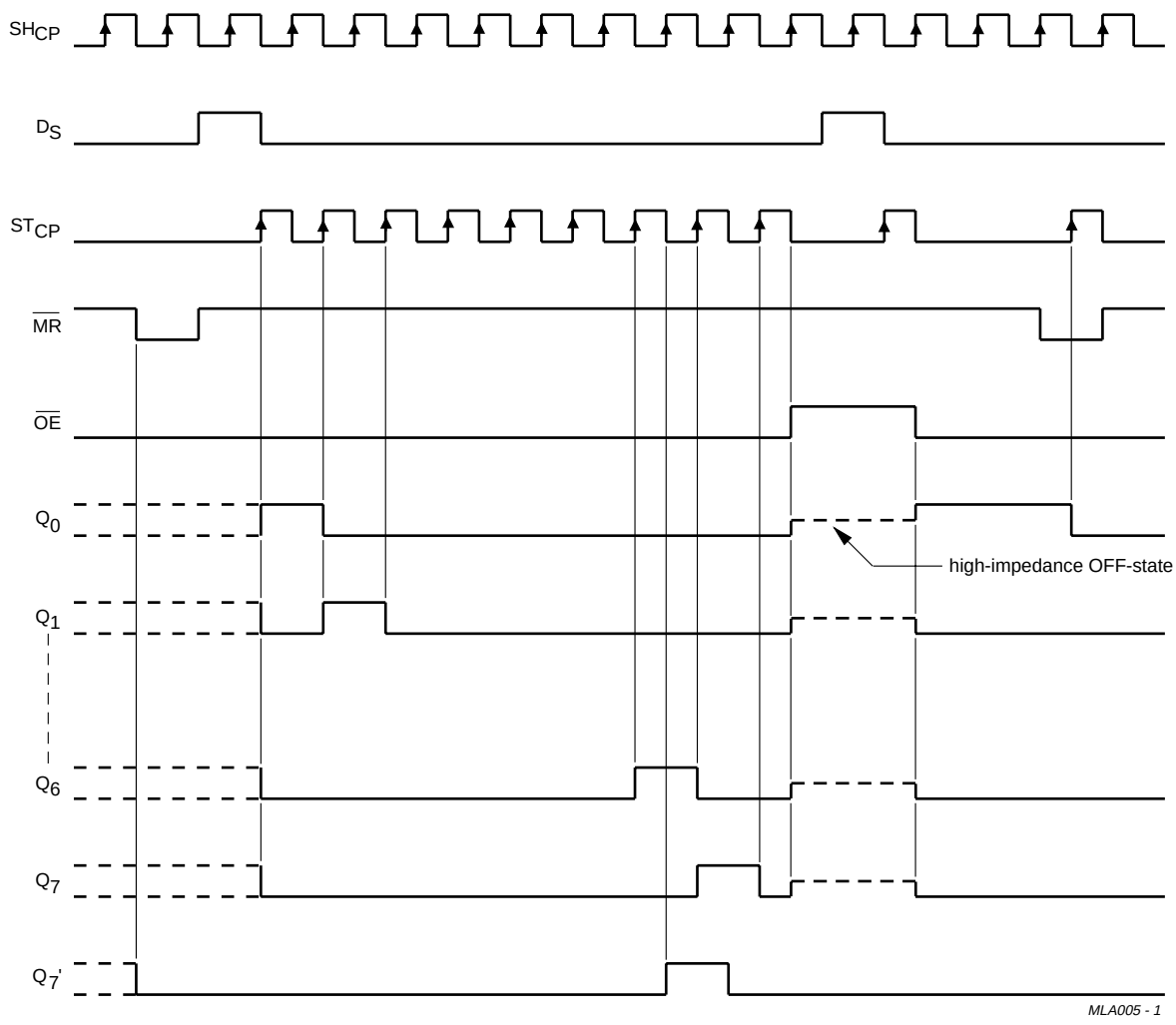



Fig.6 Timing diagram.

### DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: parallel outputs, bus driver, serial output, standard $I_{CC}$ category: MSI.

### AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF.

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITION | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | +25 | | | −40 to +85 | | −40 to +125 | | | $V_{CC}$ (V) | WAVEFORMS |
| | | min | typ | max | min | max | min | max | | | |
| $t_{PHL}/t_{PLH}$ | propagation delay $SH_{CP}$ to $Q_7$' | – | 52 | 160 | – | 200 | – | 240 | ns | 2.0 | Fig.7 |
| | | – | 19 | 32 | – | 40 | – | 48 | | 4.5 | |
| | | – | 15 | 27 | – | 34 | – | 41 | | 6.0 | |
| $t_{PHL}/t_{PLH}$ | propagation delay $ST_{CP}$ to $Q_n$ | – | 55 | 175 | – | 220 | – | 265 | ns | 2.0 | Fig.8 |
| | | – | 20 | 35 | – | 44 | – | 53 | | 4.5 | |
| | | – | 16 | 30 | – | 37 | – | 45 | | 6.0 | |
| $t_{PHL}$ | propagation delay $\overline{MR}$ to $Q_7$' | – | 47 | 175 | – | 220 | – | 265 | ns | 2.0 | Fig.10 |
| | | – | 17 | 35 | – | 44 | – | 53 | | 4.5 | |
| | | – | 14 | 30 | – | 37 | – | 45 | | 6.0 | |
| $t_{PZH}/t_{PZL}$ | 3-state output enable time $\overline{OE}$ to $Q_n$ | – | 47 | 150 | – | 190 | – | 225 | ns | 2.0 | Fig.11 |
| | | – | 17 | 30 | – | 38 | – | 45 | | 4.5 | |
| | | – | 14 | 26 | – | 33 | – | 38 | | 6.0 | |
| $t_{PHZ}/t_{PLZ}$ | 3-state output disable time $\overline{OE}$ to $Q_n$ | – | 41 | 150 | – | 190 | – | 225 | ns | 2.0 | Fig.11 |
| | | – | 15 | 30 | – | 38 | – | 45 | | 4.5 | |
| | | – | 12 | 26 | – | 33 | – | 38 | | 6.0 | |
| $t_W$ | shift clock pulse width HIGH or LOW | 75 | 17 | – | 95 | – | 110 | – | ns | 2.0 | Fig.7 |
| | | 15 | 6 | – | 19 | – | 22 | – | | 4.5 | |
| | | 13 | 5 | – | 16 | – | 19 | – | | 6.0 | |
| $t_W$ | storage clock pulse width HIGH or LOW | 75 | 11 | – | 95 | – | 110 | – | ns | 2.0 | Fig.8 |
| | | 15 | 4 | – | 19 | – | 22 | – | | 4.5 | |
| | | 13 | 3 | – | 16 | – | 19 | – | | 6.0 | |
| $t_W$ | master reset pulse width LOW | 75 | 17 | – | 95 | – | 110 | – | ns | 2.0 | Fig.10 |
| | | 15 | 6.0 | – | 19 | – | 22 | – | | 4.5 | |
| | | 13 | 5.0 | – | 16 | – | 19 | – | | 6.0 | |
| $t_{su}$ | set-up time $D_S$ to $SH_{CP}$ | 50 | 11 | – | 65 | – | 75 | – | ns | 2.0 | Fig.9 |
| | | 10 | 4.0 | – | 13 | – | 15 | – | | 4.5 | |
| | | 9.0 | 3.0 | – | 11 | – | 13 | – | | 6.0 | |
| $t_{su}$ | set-up time $SH_{CP}$ to $ST_{CP}$ | 75 | 22 | – | 95 | – | 110 | – | ns | 2.0 | Fig.8 |
| | | 15 | 8 | – | 19 | – | 22 | – | | 4.5 | |
| | | 13 | 7 | – | 16 | – | 19 | – | | 6.0 | |

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITION | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | +25 | | | −40 to +85 | | −40 to +125 | | | $V_{CC}$ (V) | WAVEFORMS |
| | | min | typ | max | min | max | min | max | | | |
| $t_h$ | hold time $D_S$ to $SH_{CP}$ | 3 | −6 | – | 3 | – | 3 | – | ns | 2.0 | Fig.9 |
| | | 3 | −2 | – | 3 | – | 3 | – | | 4.5 | |
| | | 3 | −2 | – | 3 | – | 3 | – | | 6.0 | |
| $t_{rem}$ | removal time $\overline{MR}$ to $SH_{CP}$ | 50 | −19 | – | 65 | – | 75 | – | ns | 2.0 | Fig.10 |
| | | 10 | −7 | – | 13 | – | 15 | – | | 4.5 | |
| | | 9 | −6 | – | 11 | – | 13 | – | | 6.0 | |
| $f_{max}$ | maximum clock pulse frequency $SH_{CP}$ or $ST_{CP}$ | 9 | 30 | – | 4.8 | – | 4 | – | MHz | 2.0 | Figs 7 and 8 |
| | | 30 | 91 | – | 24 | – | 20 | – | | 4.5 | |
| | | 35 | 108 | – | 28 | – | 24 | – | | 6.0 | |

### DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: parallel outputs, bus driver; serial output, standard $I_{CC}$ category: MSI.

### Note to HCT types

The value of additional quiescent supply current ($\Delta I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\Delta I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF.

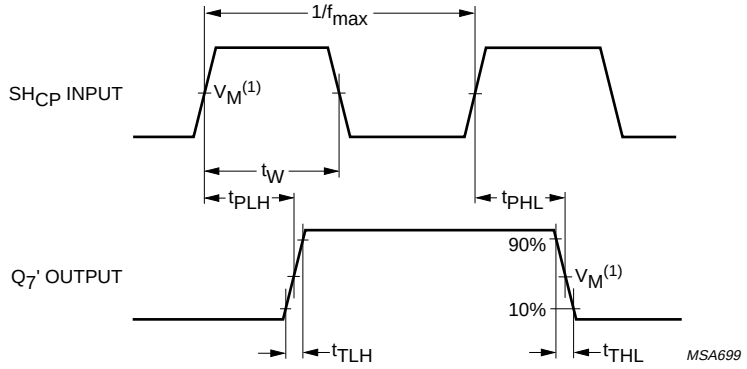
| INPUT | UNIT LOAD COEFFICIENT |
|---|---|
| $D_S$ | 0.25 |
| $\overline{MR}$ | 1.50 |
| $SH_{CP}$ | 1.50 |
| $ST_{CP}$ | 1.50 |
| $\overline{OE}$ | 1.50 |

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF.

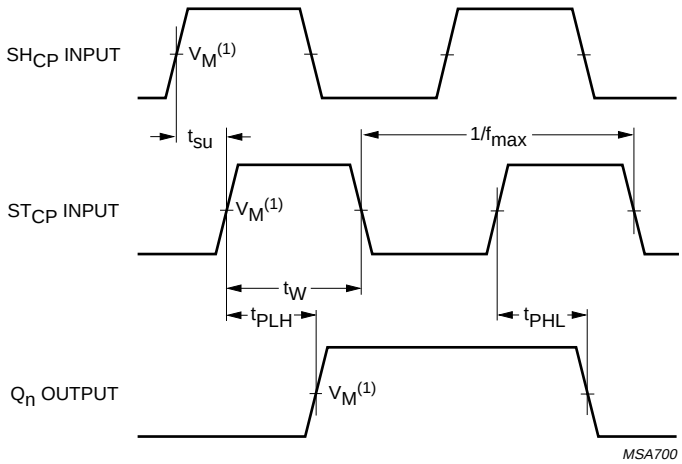
| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITION | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | +25 | | | −40 to +85 | | −40 to +125 | | | $V_{CC}$ (V) | WAVEFORMS |
| | | min | typ | max | min | max | min | max | | | |
| $t_{PHL}/ t_{PLH}$ | propagation delay $SH_{CP}$ to $Q_7$' | – | 25 | 42 | – | 53 | – | 63 | ns | 4.5 | Fig.7 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $ST_{CP}$ to $Q_n$ | – | 24 | 40 | – | 50 | – | 60 | ns | 4.5 | Fig.8 |
| $t_{PHL}$ | propagation delay $\overline{MR}$ to $Q_7$' | – | 23 | 40 | – | 50 | – | 60 | ns | 4.5 | Fig.10 |
| $t_{PZH}/ t_{PZL}$ | 3-state output enable time $\overline{OE}$ to $Q_n$ | – | 21 | 35 | – | 44 | – | 53 | ns | 4.5 | Fig.11 |
| $t_{PHZ}/ t_{PLZ}$ | 3-state output disable time $\overline{OE}$ to $Q_n$ | – | 18 | 30 | – | 38 | – | 45 | ns | 4.5 | Fig.11 |
| $t_W$ | shift clock pulse width HIGH or LOW | 16 | 6 | – | 20 | – | 24 | – | ns | 4.5 | Fig.7 |
| $t_W$ | storage clock pulse width HIGH or LOW | 16 | 5 | – | 20 | – | 24 | – | ns | 4.5 | Fig.8 |
| $t_W$ | master reset pulse width LOW | 20 | 8 | – | 25 | – | 30 | – | ns | 4.5 | Fig.10 |
| $t_{su}$ | set-up time $D_S$ to $SH_{SP}$ | 16 | 5 | – | 20 | – | 24 | – | ns | 4.5 | Fig.9 |
| $t_{su}$ | set-up time $SH_{CP}$ to $ST_{CP}$ | 16 | 8 | – | 20 | – | 24 | – | ns | 4.5 | Fig.8 |
| $t_h$ | hold time $D_S$ to $SH_{CP}$ | 3 | −2 | – | 3 | – | 3 | – | ns | 4.5 | Fig.9 |
| $t_{rem}$ | removal time $\overline{MR}$ to $SH_{CP}$ | 10 | −7 | – | 13 | – | 15 | – | ns | 4.5 | Fig.10 |
| $f_{max}$ | maximum clock pulse frequency $SH_{CP}$ or $ST_{CP}$ | 30 | 52 | – | 24 | – | 20 | – | MHz | 4.5 | Figs 7 and 8 |

**AC WAVEFORMS**



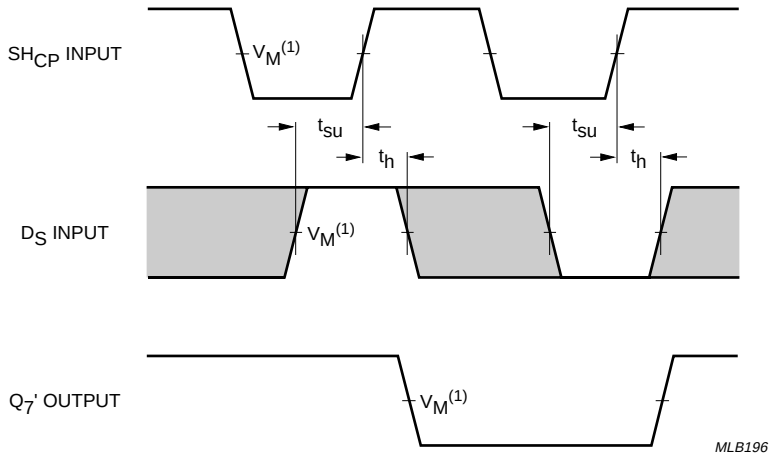

(1) HC: $V_M$ = 50%; $V_I$ = GND to $V_{CC}$
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.7 Waveforms showing the clock ($SH_{CP}$) to output ($Q_7$') propagation delays, the shift clock pulse width and maximum shift clock frequency.



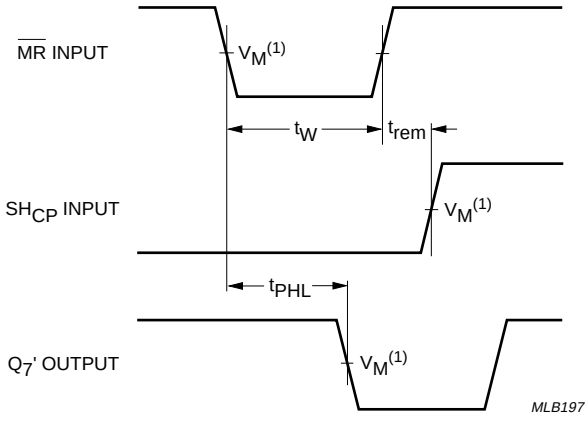

(1) HC: $V_M$ = 50%; $V_I$ = GND to $V_{CC}$
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.8 Waveforms showing the storage clock ($ST_{CP}$) to output ($Q_n$) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time.



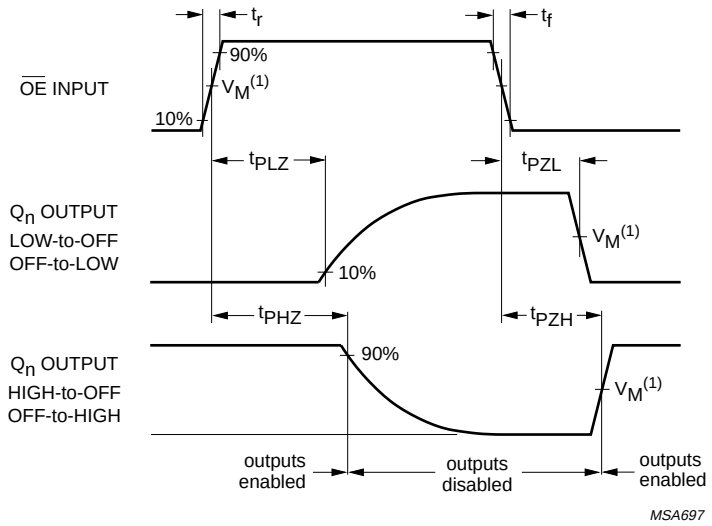

(1) HC: $V_M$ = 50%; $V_I$ = GND to $V_{CC}$
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.9 Waveforms showing the data set-up and hold times for the $D_S$ input.




(1) HC: $V_M$ = 50%; $V_I$ = GND to $V_{CC}$
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.10 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output ($Q_7$') propagation delay and the master reset to shift clock ($SH_{CP}$) removal time.




(1) HC: $V_M$ = 50%; $V_I$ = GND to $V_{CC}$
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.11 Waveforms showing the 3-state enable and disable times for input $\overline{OE}$.